Copyright 1986-2016 Xilinx, Inc. All Rights Reserved.

-----------------------------------------------------------------------------------------------------

| Tool Version : Vivado v.2016.2 (win64) Build 1577090 Thu Jun 2 16:32:40 MDT 2016

| Date : Sat Oct 21 17:28:21 2017

| Host : DESKTOP-B4BN76U running 64-bit major release (build 9200)

| Command : report\_utilization -file sort\_utilization\_placed.rpt -pb sort\_utilization\_placed.pb

| Design : sort

| Device : 7a35tcsg324-1

| Design State : Fully Placed

-----------------------------------------------------------------------------------------------------

Utilization Design Information

Table of Contents

-----------------

1. Slice Logic

1.1 Summary of Registers by Type

2. Slice Logic Distribution

3. Memory

4. DSP

5. IO and GT Specific

6. Clocking

7. Specific Feature

8. Primitives

9. Black Boxes

10. Instantiated Netlists

1. Slice Logic

--------------

+-------------------------+------+-------+-----------+-------+

| Site Type | Used | Fixed | Available | Util% |

+-------------------------+------+-------+-----------+-------+

| Slice LUTs | 296 | 0 | 20800 | 1.42 |

| LUT as Logic | 296 | 0 | 20800 | 1.42 |

| LUT as Memory | 0 | 0 | 9600 | 0.00 |

| Slice Registers | 160 | 0 | 41600 | 0.38 |

| Register as Flip Flop | 160 | 0 | 41600 | 0.38 |

| Register as Latch | 0 | 0 | 41600 | 0.00 |

| F7 Muxes | 0 | 0 | 16300 | 0.00 |

| F8 Muxes | 0 | 0 | 8150 | 0.00 |

+-------------------------+------+-------+-----------+-------+

1.1 Summary of Registers by Type

--------------------------------

+-------+--------------+-------------+--------------+

| Total | Clock Enable | Synchronous | Asynchronous |

+-------+--------------+-------------+--------------+

| 0 | \_ | - | - |

| 0 | \_ | - | Set |

| 0 | \_ | - | Reset |

| 0 | \_ | Set | - |

| 0 | \_ | Reset | - |

| 0 | Yes | - | - |

| 0 | Yes | - | Set |

| 0 | Yes | - | Reset |

| 0 | Yes | Set | - |

| 160 | Yes | Reset | - |

+-------+--------------+-------------+--------------+

2. Slice Logic Distribution

---------------------------

+------------------------------------------+------+-------+-----------+-------+

| Site Type | Used | Fixed | Available | Util% |

+------------------------------------------+------+-------+-----------+-------+

| Slice | 125 | 0 | 8150 | 1.53 |

| SLICEL | 91 | 0 | | |

| SLICEM | 34 | 0 | | |

| LUT as Logic | 296 | 0 | 20800 | 1.42 |

| using O5 output only | 0 | | | |

| using O6 output only | 128 | | | |

| using O5 and O6 | 168 | | | |

| LUT as Memory | 0 | 0 | 9600 | 0.00 |

| LUT as Distributed RAM | 0 | 0 | | |

| LUT as Shift Register | 0 | 0 | | |

| LUT Flip Flop Pairs | 24 | 0 | 20800 | 0.12 |

| fully used LUT-FF pairs | 24 | | | |

| LUT-FF pairs with one unused LUT | 0 | | | |

| LUT-FF pairs with one unused Flip Flop | 0 | | | |

| Unique Control Sets | 1 | | | |

+------------------------------------------+------+-------+-----------+-------+

\* Note: Review the Control Sets Report for more information regarding control sets.

3. Memory

---------

+----------------+------+-------+-----------+-------+

| Site Type | Used | Fixed | Available | Util% |

+----------------+------+-------+-----------+-------+

| Block RAM Tile | 0 | 0 | 50 | 0.00 |

| RAMB36/FIFO\* | 0 | 0 | 50 | 0.00 |

| RAMB18 | 0 | 0 | 100 | 0.00 |

+----------------+------+-------+-----------+-------+

\* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

4. DSP

------

+-----------+------+-------+-----------+-------+

| Site Type | Used | Fixed | Available | Util% |

+-----------+------+-------+-----------+-------+

| DSPs | 0 | 0 | 90 | 0.00 |

+-----------+------+-------+-----------+-------+

5. IO and GT Specific

---------------------

+-----------------------------+------+-------+-----------+-------+

| Site Type | Used | Fixed | Available | Util% |

+-----------------------------+------+-------+-----------+-------+

| Bonded IOB | 161 | 161 | 210 | 76.67 |

| IOB Master Pads | 77 | | | |

| IOB Slave Pads | 78 | | | |

| Bonded IPADs | 0 | 0 | 2 | 0.00 |

| PHY\_CONTROL | 0 | 0 | 5 | 0.00 |

| PHASER\_REF | 0 | 0 | 5 | 0.00 |

| OUT\_FIFO | 0 | 0 | 20 | 0.00 |

| IN\_FIFO | 0 | 0 | 20 | 0.00 |

| IDELAYCTRL | 0 | 0 | 5 | 0.00 |

| IBUFDS | 0 | 0 | 202 | 0.00 |

| PHASER\_OUT/PHASER\_OUT\_PHY | 0 | 0 | 20 | 0.00 |

| PHASER\_IN/PHASER\_IN\_PHY | 0 | 0 | 20 | 0.00 |

| IDELAYE2/IDELAYE2\_FINEDELAY | 0 | 0 | 250 | 0.00 |

| ILOGIC | 0 | 0 | 210 | 0.00 |

| OLOGIC | 0 | 0 | 210 | 0.00 |

+-----------------------------+------+-------+-----------+-------+

6. Clocking

-----------

+------------+------+-------+-----------+-------+

| Site Type | Used | Fixed | Available | Util% |

+------------+------+-------+-----------+-------+

| BUFGCTRL | 1 | 0 | 32 | 3.13 |

| BUFIO | 0 | 0 | 20 | 0.00 |

| MMCME2\_ADV | 0 | 0 | 5 | 0.00 |

| PLLE2\_ADV | 0 | 0 | 5 | 0.00 |

| BUFMRCE | 0 | 0 | 10 | 0.00 |

| BUFHCE | 0 | 0 | 72 | 0.00 |

| BUFR | 0 | 0 | 20 | 0.00 |

+------------+------+-------+-----------+-------+

7. Specific Feature

-------------------

+-------------+------+-------+-----------+-------+

| Site Type | Used | Fixed | Available | Util% |

+-------------+------+-------+-----------+-------+

| BSCANE2 | 0 | 0 | 4 | 0.00 |

| CAPTUREE2 | 0 | 0 | 1 | 0.00 |

| DNA\_PORT | 0 | 0 | 1 | 0.00 |

| EFUSE\_USR | 0 | 0 | 1 | 0.00 |

| FRAME\_ECCE2 | 0 | 0 | 1 | 0.00 |

| ICAPE2 | 0 | 0 | 2 | 0.00 |

| PCIE\_2\_1 | 0 | 0 | 1 | 0.00 |

| STARTUPE2 | 0 | 0 | 1 | 0.00 |

| XADC | 0 | 0 | 1 | 0.00 |

+-------------+------+-------+-----------+-------+

8. Primitives

-------------

+----------+------+---------------------+

| Ref Name | Used | Functional Category |

+----------+------+---------------------+

| FDRE | 160 | Flop & Latch |

| LUT5 | 136 | LUT |

| LUT3 | 136 | LUT |

| LUT6 | 128 | LUT |

| IBUF | 81 | IO |

| OBUF | 80 | IO |

| LUT4 | 64 | LUT |

| CARRY4 | 20 | CarryLogic |

| BUFG | 1 | Clock |

+----------+------+---------------------+

9. Black Boxes

--------------

+----------+------+

| Ref Name | Used |

+----------+------+

10. Instantiated Netlists

-------------------------

+----------+------+

| Ref Name | Used |

+----------+------+